



OPERATION, COMPARE, BRANCH VLIW PROCESSOR

INTRODUCTION

A VLIW processor is provided with an architecture, which includes fetching and executing circuitry, that when combined with operation, compare, branch (OCB) instructions realizes no processing branch penalties. The OCB instructions are provided with two direct branch fields or with two indirect branch fields.

CONCEPT

The technology eliminates branch penalties from pipeline microprocessors, therefore improving digital signal processing capabilities. The performance of all current pipeline microprocessors is limited by branch (or jump) instructions. The execution asymmetry of a branch (or jump) instruction can cause a stall in the microprocessor's pipeline. When a branch is taken, the next instruction is not in the execution pipeline and a pipeline stall or branch penalty occurs.

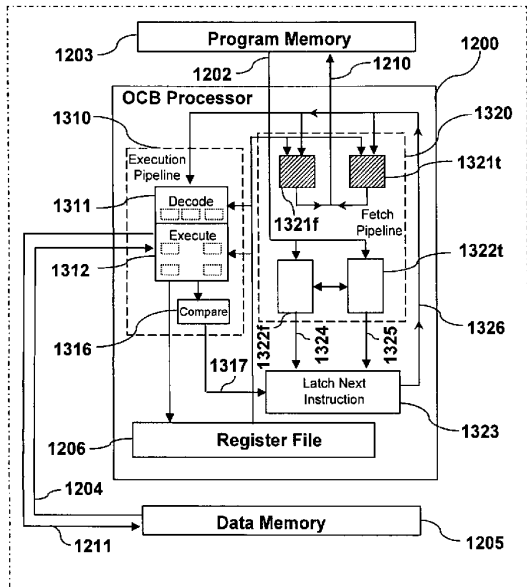
POTENTIAL MARKET

- Microprocessors and computer hardware Industries

DOING BUSINESS WITH CCDC AVIATION & MISSILE CENTER

CCDC Aviation & Missile Center is a leader in partnering with domestic firms. Successfully developed and implemented innovative tools to ease the technology transfer process such as:

- Patent License Agreements
- Cooperative Research and Development Agreements
- Test Services Agreements



INVENTION OVERVIEW

- Improved digital signal processing performance in applications where there are a large number of complex decision and comparison.
- U.S. Patent Number: 7,818,552 B2
- Application Number: 11/960,932
- Date of Patent: 19 Oct 2010

FOR FURTHER INFORMATION:

U.S. ARMY COMBAT CAPABILITIES DEVELOPMENT
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